Patent
Attorney's Docket No. F0255

AF/B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Feng-Jong Edward Yang et al.	)	Group Art Unit: 2155
	)	
Application No.: 09/650,195	)	Examiner: K. Bates
	)	
Filed: August 29, 2000	)	
	)	
For: METHOD AND APPARATUS FOR ACCESSING EXTERNAL MEMORIES	)	

TRANSMITTAL FOR APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Appeal Brief-Patents
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Transmitted herewith is an Appeal Brief in support of the Notice of Appeal filed December 2, 2004.

Enclosed is a check for ☐ $250.00 ☒ $500.00 to cover the Government fee.

The Commissioner is hereby authorized to charge any other appropriate fees that may be required by this paper that are not accounted for above, and to credit any overpayment, to Deposit Account No. 50-1070.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: _____
Glenn Snyder
Reg. No. 41,428

11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800
CUSTOMER NUMBER: 45114
Date: February 2, 2005

PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Feng-Jong Edward Yang et al.	)	Group Art Unit: 2155
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APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Window, Mail Stop Appeal Brief - Patents
Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

Sir:

This Appeal Brief is submitted in response to the rejection mailed September 3, 2004 and in support of the Notice of Appeal filed December 2, 2004.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals, interferences or judicial proceedings.

III. STATUS OF CLAIMS

Claims 1-7, 9-13 and 15-19 are pending in this application. Claims 8, 14 and 20 have been previously canceled without prejudice or disclaimer. All of the pending claims are the subject of the present appeal.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the Final Office Action mailed September 3, 2004.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Each of the independent claims involved in this appeal is recited below, followed in parenthesis by examples of where support can be found in the specification and drawings for the claimed subject matter. In addition, each dependent claim argued separately below is also summarized in a similar manner.

Claim 1 recites : A network device configured to control communication of data frames between stations (page 3, line 30 to page 4, line 8, Fig. 1, 110), comprising: a plurality of receive devices corresponding to ports on the network device, the receive devices configured to receive data frames from the stations (page 4, lines 9-21, Fig. 1, 120 and 130); and an external memory interface (Fig. 2, 140) configured to receive data from the plurality of receive devices, transfer a portion of the data received from a first one of the receive devices to a first

memory (Fig. 2, 150), and transfer a portion of the data received from a second one of the receive devices to a second memory (Fig. 2, 160), the external memory interface including a first external memory bus (Fig. 2, 170) to transfer data to the first memory and a second external memory bus (Fig. 2, 180) to transfer data to the second memory, the external memory interface being further configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus (page 6, last paragraph, Fig. 4).

Claim 10 recites: In a network device that controls communication of data frames between stations, a method of storing data frame information, comprising: receiving a plurality of data frames (page 5, lines 25-26, Fig. 3, 310); temporarily storing the received data frames in a plurality of receive devices (page 5, lines 26-27, Fig. 3, 320); and simultaneously transferring data frame information to at least a first memory and a second memory (page 6, lines 17-21, Fig. 3, 350), wherein the simultaneously transferring includes: alternately transferring data frame information from a first group of the receive devices to the first and second memories, and alternately transferring data frame information from a second group of the receive devices to the first and second memories (page 7, lines 1-10, page 8, lines 8-14, Fig. 3, 360 and Fig. 5).

Claim 16 recites: A data communication system for controlling the communication of data frames between stations, comprising: a plurality of receive devices configured to receive

data frames from the stations (page 4, lines 9-21, Fig. 1, 120 and 130); a scheduler coupled to the plurality of receive devices and configured to generate selection signals to selectively output data frame information from the receive devices (page 5, lines 13-22, Fig. 2, 230); a switching device configured to receive the data frame information and to simultaneously transfer data frame information from a first one of the data frames via a first external memory bus and data frame information from a second one of the data frames via a second external memory bus (page 6, lines 17-21, Fig. 2, 240); a first memory (Fig. 2, 150) configured to receive data frame information from the first external memory bus (Fig. 2, 170); and a second memory (Fig. 2, 160) configured to receive data frame information from the second external memory bus (Fig. 2, 180), wherein the switching device is further configured to: generate data address information having odd addresses for data transferred to the first memory and generate data address information having even addresses for data transferred to the second memory (page 6, last paragraph, Fig. 4).

Claim 2 recites: The network device of claim 1, wherein the external memory interface includes: a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories (Fig. 2, 230), the scheduler simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, respectively (page 6, lines 9-16).

Claim 4 recites: The network device of claim 1, wherein the external memory interface is further configured to simultaneously transfer the portions of the data from the first and second receive devices to the first and second memories (page 6, lines 17-21).

Claim 6 recites: The network device of claim 5, wherein the external memory interface is further configured to alternately transfer data received from the first group of receive devices to the first and second memories and to alternately transfer data received from the second group of receive devices to the first and second memories (page 7, lines 1-10, page 8, lines 8-14 and Fig. 5).

Claim 7 recites: The network device of claim 5, wherein the first and second external memory buses are each 8-bytes wide and operate at a frequency of 100 MHz (page 8, lines 27-30).

Claim 11 recites: The method of claim 10, further comprising: simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices (page 6, lines 9-16, Fig. 3, 330).

Claim 17 recites: The system of claim 16, further comprising: first and second multiplexers (Fig. 2, 210 and 220) coupled to first and second groups of the receive devices,

respectively, each of the first and second multiplexers being configured to receive the selection signals from the scheduler and to output a portion of a data frame (page 6, lines 7-16).

Claim 18 recites: The system of claim 17, wherein the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory buses (page 7, lines 1-10, page 8, lines 8-14, Fig. 3, 360 and Fig. 5).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 9-11, 13 and 15-19 have been rejected under 35 U.S.C. § 103 (a) as being unpatentable over Hassell et al. (U.S. Patent No. 6,208,650; hereinafter Hassell) in view of Springer et al. (U.S. Patent No. 4,247,920; hereinafter Springer).

B. Claims 2-6 and 12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hassell in view of Springer and further in view of Gayton et al. (U.S. Patent No. 5,680,401; hereinafter Gayton).

C. Claim 7 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hassell in view of Springer in view of Gayton and further in view of Runaldue et al. (U.S. Patent No. 6,052,751; hereinafter Runaldue).

VII. ARGUMENT

A. Rejection under 35 U.S.C. § 103 based on Hassell in view of Springer

1. Claims 1 and 9

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been realistically motivated to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing the requisite motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or to combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 USPQ 543 (Fed. Cir. 1985). Consistent legal precedent admonishes against the indiscriminate combination of prior art references. Carella v. Starlight Archery, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281,

227 USPQ 657 (Fed. Cir. 1985).

With these principles in mind, claim 1 recites a network device that includes a plurality of receive devices and an external memory interface. The external memory interface is configured to receive data from the plurality of receive devices, transfer a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory, the external memory interface including a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory, the external memory interface being further configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus.

The Final Office Action admits that Hassell does not disclose an external memory interface as recited in claim 1 (Final Office Action – pages 2-3). The Final Office Action, however, states that Springer discloses an external memory interface that includes an even memory and an odd memory and points to col. 1, lines 63-67 for support (Final Office Action – page 3). The Final Office Action further states that Springer discloses that the external memory interface includes a first external memory bus and a second external memory bus and that the external memory interface is configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus and points to col. 5, line 34 to col. 6, line 6 for support (Final Office Action – page 3). Appellants respectfully disagree.

Initially, Appellants note that it is not clear what element(s) in Springer are alleged to be equivalent to the claimed external memory interface. Appellants pointed this out in the Request for Reconsideration filed November 3, 2004. The Advisory Action mailed November 23, 2004, however, provided no clarification. In any event, Springer does not disclose or suggest the claimed external memory interface, as discussed in detail below.

Springer is directed to a system for permitting individual bytes of a two-byte information signal to be stored or retrieved from a single memory space (Springer – col. 1, lines 40-58). Springer at col. 1, lines 63-67 discloses that a memory device may be divided into two modules, one designated odd and the other designated even to indicate a logical grouping of addresses. Springer at col. 5, line 6 to col. 6, line 6 discloses performing a 16-bit memory access to memory modules 22 and 24 (Fig. 1). Springer discloses that a 16-bit memory access will result in an access to both modules 22 and 24 at a module address of N/2 if N is even and access to module 22 at an address defined by an integer part of N/2 and an access to module 24 at an address defined by the integer part of (N+1)/2 if N is odd (col. 5, lines 27-33 and Fig. 1). Therefore, Springer discloses that access to modules 22 and 24 is based on receipt of an address signal N on address signal line 34 (See col. 2, lines 60-68 and Fig. 1).

Springer is clearly not directed to transferring data from receive devices that correspond to ports on a network device. Springer, therefore, cannot disclose an external memory interface that transfers data received from a first receive device (that corresponds to a

port) to a first memory and transfers data received from a second receive device (that corresponds to a port) to a second memory, as required by claim 1.

Springer further does not disclose an external memory interface that is configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus. Springer, in contrast, merely discloses that the system of Fig. 1 provides access to even or odd memory based on an address on signal line 34.

In response to similar arguments made in a previous response, the Final Office Action states that Springer discloses "the ability to write 8 bit data addressed to an odd memory space into an odd memory, to write 8 bit data addressed to even memory into an even memory, and to write a 16 bit word into 8 bit additions to the even and odd memories" and points to col. 5, lines 37-53 and Figs. 1 and 2 for support (Final Office Action – pages 8-9). The Final Office Action further states that "when the scheduler stores odd addressed data, that data gets sent across the memory bus that corresponds to odd memory, and the same with even addressed memory, this is the same as generating odd address information via the first memory bus as seen in the specification on page 7, line 24 to page 8, line 7" (Final Office Action – page 9). Appellants respectfully disagree.

Writing odd addressed words into an odd address memory and even addressed words into an even memory, as disclosed by Springer, is simply not equivalent to and does not suggest the use of an external memory interface that is configured to receive data from a plurality of receive devices (where the receive devices are configured to receive data frames

from stations and the receive devices correspond to ports on a network device) and generate odd address information when transferring data via a first external memory bus and generate even address information when transferring data via a second external memory bus. That is, the mere use of odd addresses and even addresses, as disclosed in Springer, does not disclose or suggest the use of an external memory interface, as recited in claim 1.

For at least theses reasons, the combination of Hassell and Springer does not disclose or suggest each of the features of claim 1.

In addition, even if, for the sake of argument, the combination of Hassell and Springer could be fairly construed to disclose or suggest each of the features of claim 1, the Final Office Action does not provide the requisite motivation under 35 U.S.C. § 103 as to why it would have been obvious to combine Hassell and Springer.

For example, the Final Office Action states that it would have been obvious to use Springer's teaching in Hassell's switch "in order to have memory modules that are accessible in parallel (Column 1, lines 63-65) without having a more complex addressing system (Column 2, lines 28-33)" (Final Office Action – page 3). Appellants respectfully disagree.

Hassell is directed to a circuit for performing high-speed low latency frame relay switching (Hassell – Abstract). Springer, in contrast, is directed to a method for permitting the transfer of a two-byte information signal into and out of a storage area (Springer – Abstract). These two references are unrelated, other than the fact that both may include memory devices, and are clearly directed to totally different areas of technology. The Examiner's alleged motivation for combining these disparate references is merely a conclusory statement providing

an alleged benefit of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103.

Further, the portions of Springer to which the Final Office Action points, apparently as providing motivation for the combination, (i.e., col. 1, lines 63-65 and col. 2, lines 28-33) merely disclose that a memory device is divided into two parallel accessible modules and that transferring a two-byte signal may be accomplished without regard to whether the first bytes being addressed are odd or even. These portions of Springer also do not provide objective motivation as to why it would have been obvious to combine Springer with Hassell.

In response to similar arguments made in the Request for Reconsideration filed November 3, 2004, the Advisory Action mailed November 23, 2004 states that the combination leads to improve Hassell's external memory by having separate external memory modules that can be addressed and accessed separately by having separate data paths, or in this case data buses (Advisory Action – continuation sheet). The Advisory Action also states that there is also motivation to make the combination because Springer allows two memory modules to work as a single large memory unit, allowing parallel writes, while also working as two separate memory modules allowing separate accesses to each and points to col. 1, lines 63-65 and col. 6, lines 54-59 for support (Advisory Action – continuation sheet). Appellants respectfully disagree.

Once again, the alleged motivation for combining Springer with Hassell amounts to a conclusory statement regarding an alleged benefit of the combination. Springer at col. 1, lines 63-65, as discussed above, discloses that a memory device may be divided into two parallel

accessible modules, one designated odd and the other even. Springer at col. 6, lines 54-59 discloses an 8-bit access mode for the system of Fig. 4 in which a read or write signal and the address of the memory location are impressed on signal lines 150, 151, 152 and 134, respectively. Control circuit 138 disables address incrementer 136 and causes the upper 15 bits of the address signal to be passed to both memory modules 122 and 124 and the least significant bits to be passed to the control circuit 138. It is not clear how either of these portions of Hassell could be construed as providing objective motivation as to why it would have been obvious to combine features from a memory access system, as disclosed in Springer, with Hassell, which is directed to a low latency frame relay switching system. As discussed above, Appellants assert that the two references are unrelated, other than the fact that both may include memories. The mere fact that one reference allegedly provides a missing teaching with respect to a claim does not provide objective motivation as to why it would have been obvious to combine otherwise unrelated references.

For at least these reasons, Appellants respectfully submit that the rejection of claim 1 is improper. Accordingly, reversal of the rejection of claims 1 and 9 is respectfully requested.

2. Claims 10, 12, 13 and 15

Claim 10 recites a method for storing data frame information that includes simultaneously transferring data frame information to at least a first memory and a second memory, wherein the simultaneously transferring includes alternately transferring data frame information from a first group of the receive devices to the first and second memories and

alternately transferring data frame information from a second group of the receive devices to the first and second memories.

The Final Office Action effectively admits that Hassell does not disclose these features, but states that Springer discloses these features and points to col. 2, lines 1-11 for support (Final Office Action – page 4). Appellants respectfully disagree.

Springer at col. 2, lines 1-11 discloses:

> For an even memory address N, an access is made to a location in each memory module having an address of N/2. For an odd memory address N, the access in the odd module is to a location having an address defined by the integer part of N/2, but the access in the odd module is to a location having an address defined by the integer part of N/2+1. In the first case, the even memory module supplies or receives the upper byte of the information signal, and in the second case, the odd module supplies or receives the upper byte.

This portion of Springer merely discloses how to process an incoming address signal N with respect to an odd and even memory module. This portion of Springer clearly does not disclose alternately transferring data frame information from a first group of the receive devices to the first and second memories and alternately transferring data frame information from a second group of the receive devices to the first and second memories, as required by claim 10.

In response to a similar argument made in a previous response, the Final Office Action states that Appellants are attempting to argue the art individually and not as a combination (Final Office Action – page 9). Appellants disagree with the characterization of these arguments and maintain that the Examiner has not addressed the features recited in claim 10.

First, claim 10 recites that the simultaneously transferring includes alternately transferring data frame information from a first group of the receive devices to the first and second memories and alternately transferring data frame information from a second group of the receive devices to the first and second memories.

Springer may disclose the use of an odd and even memory, which are apparently considered by the Examiner to be equivalent to the claimed first and second memories. However, the mere fact that Springer discloses use of odd and even addressed memories cannot be fairly construed to disclose or suggest the claimed features. That is, the Final Office Action has not pointed out where Springer allegedly discloses alternately transferring data frame information from a first group of receive devices to the odd and even memories in Springer, as required by claim 10 (based on the alleged equivalence of the odd and even memories to the claimed first and second memories). The Final Office Action has also not pointed out where Springer discloses or suggests alternately transferring data frame information from a second group of receive devices to the odd and even memories in Springer, as further required by claim 10 (based on the alleged equivalence of the odd and even memories to the claimed first and second memories).

Therefore, Appellants have not argued the references individually, but merely pointed out the deficiencies in the combination of Hassell and Springer with respect to the features recited in claim 10.

The last sentence on page 9 of the Final Office Action is also unclear ("when Hassell devices to store a data frame from the first memory onto the external memory it can be sent to

both external memories simultaneously, and the same for the second receive device, thus giving the functionality of alternatively sending data from both receiving devices to both memories at once"). In any event, this statement provides no additional support for the notion that either Hassell or Springer discloses or suggests the features discussed above.

In response to similar arguments made in the Request for Reconsideration filed November 3, 2004, the Advisory Action states that Hassell allows information to be received from a first receive device and a second receive device to an external memory and Springer's improvement to the external memory allows information to be entered into the first and second memory module of memory in a 16 bit format or an 8 bit format, where the 8 bit format allows information to be addressed to either memory module, but not the other (Advisory Action – continuation sheet). The Advisory Action further states that Springer allows memory to be entered from the first group into both memory simultaneously (16 bit mode) or either memory module (8 bit mode) and this allows the first group to address information to any combination of the memory modules, which includes alternately sending data frames to both (Advisory Action – continuation sheet). Appellants respectfully disagree.

First, the Examiner has not pointed to any portion of Springer that supports the notion that Springer discloses the claimed alternately transferring recited in claim 10. Second, entering data in an 8 bit mode or a 16 bit mode cannot be construed as being equivalent to alternately transferring data frame information from a first group of the receive devices to the first and second memories and alternately transferring data frame information from a second group of the receive devices to the first and second memories, as required by claim 10.

Therefore, Springer does not disclose or suggest alternately transferring data in the manner recited in claim 10 and the Examiner's statements regarding Springer are simply not supported by the actual disclosure of Springer.

For at least these reasons, the combination of Hassell and Springer does not disclose or suggest each of the features of claim 10.

In addition, even if, for the sake of argument, the combination of Hassell and Springer could be fairly construed to disclose or suggest each of the features of claim 10, Appellants assert that the motivation to combine Hassell and Springer does not satisfy the requirements of 35 U.S.C. § 103 for the reasons discussed above with respect to claim 1.

For at least these reasons, Appellants respectfully submit that the rejection of claim 10 is improper. Accordingly, reversal of the rejection of claims 10, 12, 13 and 15 are respectfully requested.

3. Claim 11

Claim 11 recites simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices. The Final Office Action appears to admit that Hassell does not disclose this feature and relies on col. 2, lines 18-27 of Springer as allegedly disclosing this feature (Final Office Action – page 4). Appellants respectfully disagree.

Springer at col. 2, lines 18-27 discloses that an objective of Springer's invention is to provide means for transferring a two-byte information signal into and out of a byte-oriented

memory system such that the first and second bytes are associated with sequential storage locations. This portion of Springer clearly does not disclose simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices, as required by claim 11.

In response to similar arguments made in the Request for Reconsideration filed November 3, 2004, the Advisory Action states that Springer allows information to be pulled from modules separately, so having two modules and two receiving devices allows signals to be sent to the receive devices simultaneously (Advisory Action – continuation sheet). Appellants respectfully disagree.

Once again, the Examiner has not pointed to any portion of Springer supporting the notion that Springer actually discloses simultaneously transmitting selections signals to more than one memory module, as required by claim 11. Therefore, the Examiner's statement regarding simultaneously transmitting selection signals amounts to mere speculation that is not supported by the actual disclosure of Springer.

For at least these reasons, the combination of Hassell and Springer does not disclose or suggest each of the features of claim 11. Accordingly, Appellant respectfully submits that the rejection of claim 11 is improper and reversal of the rejection is respectfully requested.

4. Claims 16 and 19

Claim 16 recites a data communication system that includes a plurality of receive devices, a scheduler, a switching device, a first memory and a second memory. Claim 16

recites that the scheduler is configured to generate selection signals to selectively output data frame information from the receive devices. The Final Office Actions states that Hassell discloses this feature and points to col. 6, lines 37-52 for support (Final Office Action – page 5). Appellants respectfully disagree.

Hassell at col. 6, lines 37-52 discloses:

> The circuit has a memory management block 130 comprised of a look up table (LUT) 131 having a parameter table 132, a buffer allocation functional block 133, a buffer allocation table 134, and a free buffer pointer 136. The circuit 40 also has a frame buffer descriptor (FBD) table 140 and a queue memory 150. The queue memory 150 has an input queue 151 (shown in FIGS. 4 and 6) associated with the input queue pointer 114, an output queue 152 (shown in FIGS. 4-6) associated with the output queue pointer 121, as well as a free queue list 153 having an associated free queue pointer 154 (shown in FIG. 6).
>
> The input and output queues of the queue memory 150, and the frame buffers associated with the buffer allocation table 134 are constructed as linked lists. A linked list is a data structure in which each item of the list consists of a data component and a pointer or link to the next item in the list.

This portion of Hassell merely discloses the use of a queue memory having an input queue and an output queue. This portion of Hassell does not disclose or suggest a scheduler that is configured to generate selection signals to selectively output data frame information from the receive devices, as required by claim 16.

In response to similar arguments made in the Request for Reconsideration filed November 3, 2004, the Advisory Action states that Hassell discloses sending pointers generated for identifying locations of frames in the system, which work as a selection signal and points to col. 6, lines 63-67 for support (Advisory Action – continuation sheet). Hassell at col. 6, line 63 to col. 7, line 3 discloses that output processing block 120 receives a pointer

from output queue 152 pointed to by output queue pointer 121, receives frame relay payload data from external memory 70 through memory management block 130, process the frame's outbound header 122, buffers the assembled frame for synchronization purposes and transmits the frame using HDLC formatting 124. This portion of Hassell may disclose that an output processing block may retrieve frame payload data stored in external memory 70 for transmission. This portion of Hassell, however, does not disclose generating selection signals to selectively output data frame information from a plurality of receive devices configured to receive data frames from the stations, as required by claim 16.

Claim 16 also recites a switching device configured to receive the data frame information and to simultaneously transfer data frame information from a first one of the data frames via a first external memory bus and data frame information from a second one of the data frames via a second external memory bus. The Final Office Action states that Springer discloses these features and points to col. 2, lines 1-11 for support (Final Office Action – page 5). Appellants respectfully disagree.

As discussed above, Springer at col. 2, lines 1-11 discloses:

> For an even memory address N, an access is made to a location in each memory module having an address of N/2. For an odd memory address N, the access in the odd module is to a location having an address defined by the integer part of N/2, but the access in the odd module is to a location having an address defined by the integer part of N/2+1. In the first case, the even memory module supplies or receives the upper byte of the information signal, and in the second case, the odd module supplies or receives the upper byte.

This portion of Springer, however, does not disclose a switching device that receives data frame information (output from the receive devices), transfers data frame information

from a first data frame and transfers data frame information from a second data frame, much less that the transferring is done simultaneously. In contrast, this portion of Springer merely discloses processing associated with receiving a signal having an address N on signal line 34.

Claim 16 also recites that the switching device is further configured to generate data address information having odd addresses for data transferred to the first memory and generate data address information having even addresses for data transferred to the second memory. The Final Office Action states that Springer discloses these features and points to col. 5, line 34 to col. 6, line 6 for support (Final Office Action – page 5). Appellants respectfully disagree.

Similar to the discussion above with respect to claim 1, this portion of Springer does not disclose generating odd addresses for data transferred to a first memory and even addresses for data transferred to a second memory, as recited in claim 16. Rather, Springer merely discloses using existing address information received on address signal line 34 to determine a module address associated with accessing memory modules 22 and 24.

In response to similar arguments made in the Request for Reconsideration filed November 3, 2004, the Advisory Action states that Springer "uses the address as addressing to which module information is stored on, so it has a mux it is using as a switch device to help address where the information is to be stored" and points to Fig. 1, elements 28 and 32 for support (Advisory Action – continuation sheet). Apparently, elements 28 and 32 are considered by the Examiner to be equivalent to the claimed switching device. Appellants respectfully disagree.

Elements 28 and 32 of Springer are an input multiplexer and an output multiplexer, respectively. These multiplexers, however, do not receive data frame information and simultaneously transfer data frame information from a first data frame via a first external memory bus and data frame information from a second data frame via a second external memory bus, as required by claim 16. Multiplexers 28 and 32 also do not generate data address information having odd addresses for data transferred to a first memory and generate data address information having even addresses for data transferred to a second memory, as further required by claim 16.

Therefore, as a factual matter, the combination of Hassell and Springer does not disclose or suggest each of the features of claim 16.

In addition, even if, for the sake of argument, the combination of Hassell and Springer could be fairly construed to disclose or suggest each of the features of claim 16, Appellants assert that the motivation to combine Hassell and Springer does not satisfy the requirements of 35 U.S.C. § 103 for the reasons discussed above with respect to claim 1.

For at least these reasons, Appellants respectfully submit that the rejection of claim 16 is improper. Accordingly, reversal of the rejection of claims 16 and 19 is respectfully requested.

5. Claim 17

Claim 17 recites that the system includes first and second multiplexers coupled to first and second groups of the receive devices, respectively, each of the first and second

multiplexers being configured to receive the selection signals from the scheduler and to output a portion of a data frame. The Final Office Action states that Springer discloses these features and points to Fig. 1, elements 28, 32 and 38 for support (Final Office Action – page 5). Appellants respectfully disagree.

Elements 28 and 32 of Springer are input and output multiplexers, respectively. Element 38 is a control circuit that receives read/write signals. These elements of Springer are clearly not equivalent to first and second multiplexers coupled to first and second groups of receive devices, as required by claim 17. Further, these elements of Springer, are not configured to receive selection signals from a scheduler and output a portion of a data frame, as further required by claim 17.

For at least these reasons, Appellants respectfully submit that the rejection of claim 17 is improper. Accordingly, reversal of the rejection of claim 17 is respectfully requested.

6. Claim 18

Claim 18 recites that the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory buses. The Final Office Action states that Springer discloses this feature and points to col. 2, lines 1-11 for support (Final Office Action – page 6). Appellants respectfully disagree.

Springer at col. 2, lines 1-11, as discussed above, merely discloses how to process incoming address signals N with respect to an odd and even memory module. This portion of

Springer, however, does not even disclose the use of first and second multiplexers, much less alternately transferring data received from the first multiplexer to the first and second external memory buses and alternately transferring data received from the second multiplexer to the first and second external memory buses, as required by claim 18.

For at least these reasons, Appellants respectfully submit that the rejection of claim 18 is improper. Accordingly, reversal of the rejection of claim 18 is respectfully requested.

B. Rejection under 35 U.S.C. § 103 based on Hassell in view of Springer and further in view of Gayton

1. Claims 2 and 3

Claim 2 recites that the external memory interface includes a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories, the scheduler simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, respectively.

The Final Office Action admits that neither Hassell nor Springer discloses these features. The Final Office Action, however, states that Gayton discloses a scheduler that allows two memories to operate and deal with two different receive devices separately and simultaneously and points to col. 5, lines 16-18 for support (Final Office Action – page 6). Appellants respectfully disagree.

Gayton at col. 5, lines 16-18 discloses that TX buffer memory 46 provides 32 bits of data to TX FIFO 28 and RX buffer memory 45 reads 32 bits of data from RX FIFO 30 at

every cycle of the clock signal. This portion of Gayton, however, does not disclose a scheduler that simultaneously outputs first and second selection signals for outputting data from the first receive device and the second receive device, respectively, as recited in claim 2.

Therefore, as a factual matter, the combination of Hassell, Springer and Gayton does not disclose or suggest each of the features of claim 2.

In addition, even if, for the sake of argument, the combination of Hassell, Springer and Gayton could reasonably be construed to disclose each of the features of claim 2, the Final Office Action does not provide the requisite motivation under 35 U.S.C. § 103 as to why it would have been obvious to combine these references.

For example, the Final Office Action states that it would have been obvious to use Gayton's teaching of a plurality of external memories operating simultaneously in Hassell's switch "in order to overlap operations thus increasing throughput" and points to col. 2 lines 9-12 for support (Final Office Action – page 7). Appellants respectfully disagree.

The alleged motivation for combining Gayton with the combination of Hassell and Springer is merely a conclusory statement regarding an alleged benefit of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103. In this respect, Appellants rely upon In re Deuel, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995), wherein it was held that generalizations do not establish the realistic motivation to modify a specific reference in a specific manner to arrive at a specifically claimed invention. In addition, the portion of Gayton relied upon as providing the motivation for combining these disparate references (i.e., col. 2, lines 9-12) merely discloses that the construction of the current ATM

cells is overlapped with the management of the packet and buffer control data associated with the immediately preceding ATM cell. This portion of Gayton provides no objective motivation for combining a portion of Gayton, which is directed to a method for asynchronously segmenting packets of multiple channels into ATM cells (Gayton – Abstract) with the combination of Springer and Hassell, which are each directed to different technology areas than Gayton.

For at least these reasons, Appellants respectfully submit that the rejection of claim 2 is improper. Accordingly, reversal of the rejection of claims 2 and 3 is respectfully requested.

2. Claims 4 and 5

Claim 4 recites that the external memory interface is further configured to simultaneously transfer the portions of the data from the first and second receive devices to the first and second memories. The Final Office Action states that Gayton discloses this feature and points to col. 5, lines 16-18 for support (Final Office Action – page 7). Appellants respectfully disagree.

Gayton at col. 5, lines 16-18, as discussed above, merely discloses that TX buffer memory 46 provides 32 bits of data to TX FIFO 28 and RX buffer memory 45 reads 32 bits of data from RX FIFO 30 at every cycle. This portion of Gayton clearly does not disclose or suggest simultaneously transferring the portions of the data from the first and second receive devices to the first and second memories, as recited in claim 4.

Therefore, as a factual matter, the combination of Hassell, Springer and Gayton does not disclose or suggest each of the features of claim 4.

In addition, even if, for the sake of argument, the combination of Hassell, Springer and Gayton could reasonably be construed to disclose each of the features of claim 4, Appellants assert that the Final Office Action does not provide the requisite motivation under 35 U.S.C. § 103 as to why it would have been obvious to combine these references for reasons similar to those discussed above with respect to claim 2.

For at least these reasons, Appellants respectfully submit that the rejection of claim 4 is improper. Accordingly, reversal of the rejection of claims 4 and 5 is respectfully requested.

3. Claim 6

Claim 6 recites that the external memory interface is further configured to alternately transfer data received from the first group of receive devices to the first and second memories and to alternately transfer data received from the second group of receive devices to the first and second memories. The Final Office Action states that Springer discloses this feature and points to col. 2, lines 1-11 for support (Final Office Action – pages 7-8). Appellants respectfully disagree.

Similar to the discussion above with respect to claim 10, Springer at col. 2, lines 1-11 does not disclose or suggest alternately transferring data received from a first group of devices to the first and second memories or alternately transferring data received from a second group of devices to the first and second memories, as recited in claim 6.

Therefore, as a factual matter, the combination of Hassell, Springer and Gayton does not disclose or suggest each of the features of claim 6.

In addition, even if, for the sake of argument, the combination of Hassell, Springer and Gayton could reasonably be construed to disclose each of the features of claim 6, Appellants assert that the Final Office Action does not provide the requisite motivation under 35 U.S.C. § 103 as to why it would have been obvious to combine these references for reasons similar to those discussed above with respect to claim 2.

For at least these reasons, Appellants respectfully submit that the rejection of claim 6 is improper. Accordingly, reversal of the rejection of claim 6 is respectfully requested.

C. Rejection under 35 U.S.C. § 103 based on Hassell in view of Springer in further view of Gayton and in further view of Runaldue

1. Claim 7

Claim 7 recites that the first and second external memory buses are each 8-bytes wide and operate at a frequency of 100 MHz. The Final Office Action admits that the combination of Hassell, Springer and Gayton does not disclose this feature and relies upon Runaldue for disclosing an external memory that can operate at 100 MHz (Final Office Action – page 8). The Final Office Action states that it would have been obvious "to use Runaldue's teaching that external memory can operate at 100 MHz and enable Hassell's switch to interface with memory at that speed" (Final Office Action – page 8).

Appellants assert that even if, for the sake argument, the combination of Hassell,

Springer, Gayton and Runaldue could reasonably be construed to disclose each of the features of claim 7, the Final Office Action does not provide the requisite motivation under 35 U.S.C. § 103 as to why it would have been obvious to combine these references. That is, the alleged motivation is merely a conclusory statement regarding an alleged benefit of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103 as to why it would have been obvious to combine these four disparate references.

For at least these reasons, Appellants respectfully submit that the rejection of claim 7 is improper. Accordingly, reversal of the rejection of claim 7 is respectfully requested.

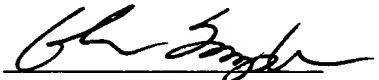
VIII. CONCLUSION

In view of the foregoing arguments, Appellants respectfully solicit the Honorable Board to reverse the Examiner's rejections of claims 1-7, 9-13 and 15-19.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: 
Glenn Snyder
Reg. No. 41,428

Date: February 2, 2005

11240 Waples Mill Road
Suite 300
Fairfax, VA 22030
Telephone: (571) 432-0800
Facsimile: (571) 432-0808

IX. APPENDIX

1. A network device configured to control communication of data frames between stations, comprising:

a plurality of receive devices corresponding to ports on the network device, the receive devices configured to receive data frames from the stations; and

an external memory interface configured to receive data from the plurality of receive devices, transfer a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory, the external memory interface including a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory, the external memory interface being further configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus.

2. The network device of claim 1, wherein the external memory interface includes:

a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories, the scheduler simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, respectively.

3. The network device of claim 2, wherein the external memory interface is further configured to simultaneously transfer 8 bytes of data from the first receive device to the first memory and 8 bytes of data from the second receive device to the second memory.

4. The network device of claim 1, wherein the external memory interface is further configured to simultaneously transfer the portions of the data from the first and second receive devices to the first and second memories.

5. The network device of claim 1, wherein the external memory interface is configured to simultaneously transfer data received from a first one of a first group of the receive devices via the first external memory bus and a second one of a second group of the receive devices via the second external memory bus.

6. The network device of claim 5, wherein the external memory interface is further configured to alternately transfer data received from the first group of receive devices to the first and second memories and to alternately transfer data received from the second group of receive devices to the first and second memories.

7. The network device of claim 5, wherein the first and second external memory buses are each 8-bytes wide and operate at a frequency of 100 MHz.

9. The network device of claim 1, wherein the external memory interface is further configured to simultaneously retrieve data from the first and second memories.

10. In a network device that controls communication of data frames between stations, a method of storing data frame information, comprising:

receiving a plurality of data frames;

temporarily storing the received data frames in a plurality of receive devices; and

simultaneously transferring data frame information to at least a first memory and a second memory, wherein the simultaneously transferring includes:

alternately transferring data frame information from a first group of the receive devices to the first and second memories, and

alternately transferring data frame information from a second group of the receive devices to the first and second memories.

11. The method of claim 10, further comprising:

simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices.

12. The method of claim 10, wherein the simultaneously transferring further includes:

transferring 8 bytes of data from a first receive device to the first memory and 8 bytes of data from a second receive device to the second memory.

13. The method of claim 10, wherein the simultaneously transferring further includes:

sending a portion of a first data frame via a first external memory bus and sending a portion of a second data frame via a second external memory bus.

15. The method of claim 10, further comprising:

simultaneously retrieving data frame information from the first and second memories.

16. A data communication system for controlling the communication of data frames between stations, comprising:

a plurality of receive devices configured to receive data frames from the stations;

a scheduler coupled to the plurality of receive devices and configured to generate selection signals to selectively output data frame information from the receive devices;

a switching device configured to receive the data frame information and to simultaneously transfer data frame information from a first one of the data frames via a first external memory bus and data frame information from a second one of the data frames via a second external memory bus;

a first memory configured to receive data frame information from the first external memory bus; and

a second memory configured to receive data frame information from the second external memory bus, wherein the switching device is further configured to:

generate data address information having odd addresses for data transferred to

the first memory and generate data address information having even addresses for data transferred to the second memory.

17. The system of claim 16, further comprising:

first and second multiplexers coupled to first and second groups of the receive devices, respectively, each of the first and second multiplexers being configured to receive the selection signals from the scheduler and to output a portion of a data frame.

18. The system of claim 17, wherein the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory buses.

19. The system of claim 16, wherein the first memory is configured to store data words having odd addresses and the second memory is configured to store data words having even addresses.